Meets HBM, MM Standards
Tests Wafer or Die

ESD and Pulse Technology

Semi-Auto ESD Tester

Model 400S Series

Model 400SW	Wafer Level ESD Tester
Model 400SC	Die Level ESD Tester

Model 400SW with Manual Wafer Prober MP-10 (MJC)

Features

- ESD Performance Test from Wafer to package
- Process Monitoring by periodical wafer test
- Allows correlation test between die location and ESD performance
- Multiple return allows ESD current path verification
- Enables rapid ESD performance test of new devices
- Decreases device development time

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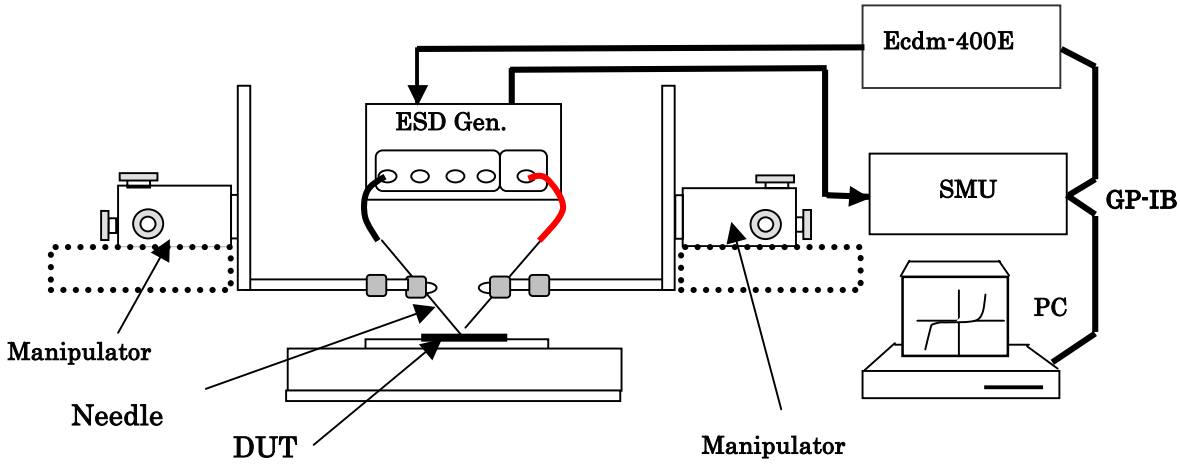
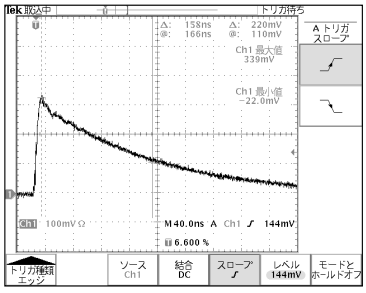
General Description

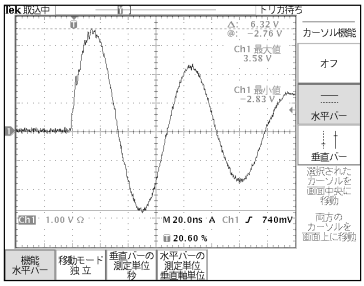
Model 400S allows zapping HBM or MM ESD stress to various shape DUT, then automatically detect damage or degradation by very little programming. Even designer simply tests the ESD performance of a new design any time.
It has been typical that ESD test is done after packaged. IC socket adaptor board is usually required to test it. This test system enables ESD test of DUT on wafer or die, so that drastic time and money saving are expected.



The universal ESD Simulator, Model Ecdm-400E, generates ESD pulse such as HBM or MM. Precise Source Measure Unit (SMU) will then detect device damage or degradation. Host PC controls pulse generation, SMU measurement and damage/degradation detection via GP-IB interface.



HBM
Waveform
(1000 V)



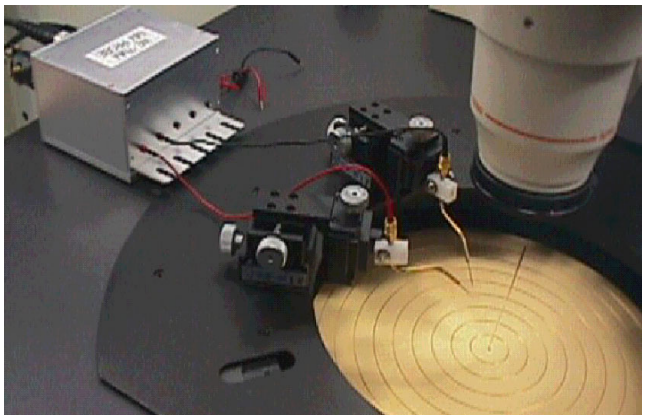
MM
Waveform
(400 V)

Semi-auto and **Automatic test** mode are included.
Semi-auto Test :V/I curves are given on the PC monitor before and after the programmed level of ESD stress. Next level of ESD stress or polarity change may be programmed watching the V/I curves so that relation between zapping parameters and device performance can be quickly verified. This is the best mode to test a device under development
Automatic Test :ESD polarity, start voltage, step voltage and damage criteria are programmed before the test. Once test is started, no operator intervention is required. This mode is suitable for developed die test, final test of the packaged device or process monitoring.

The stand alone Ecdm-400, the heart of the system, generates HBM and MM ESD pulse as well as simulates D-CDM and F-CDM tress. It is also configurable as the pulser for TLP pulse curve tracer to measure snap-back I/V curve.

Functions

1. ESD Unit and probing needles



Your manual wafer station or new station can be used for this system. Your manipulator may not be used depending the type.
Top left unit is an ESD pulse generator. It includes up to 5 current transformers to monitor one ESD current and max 4 return current so that protection device performance is accurately analyzed.

2. Monitor display

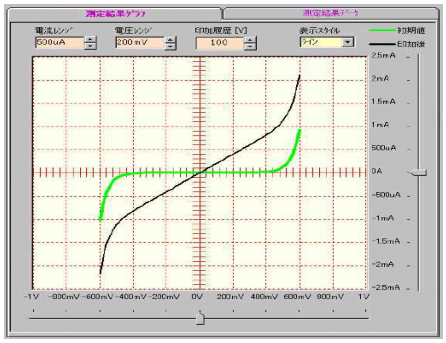
Main window for Semi-auto test

Main window for Automatic test

Semi-auto test: Three parameters are programmed any time during test

Automatic test: Parameters are programmed before starting test.

Conditions to measure V-I curve



Measured V-I curve

Max samples for V-I measurement is 91. Above 2 windows are common to Semi-auto and automatic tests. Damage criteria can be programmed in this windows. Right graph include digital data as well as curve before and after zap. Zoom up/down and zero point location can be flexibly controlled. Relation between ESD stress level and V-I curve can be shown on the monitor.

Specifications

1. Source Measure unit/Damage criteria

◇ Polarity : Positive, Negative
◇ Force Voltage
Range : 0 to 30V
Digits : 3
Minimum Step : 10mV
Tables: 4 tables (Vf-A to Vf-D)
◇ Current measurement
Range : 0 to 200mA
Digits : 3
Resolution : 10nA (*)
Averaging : 1, 2, 4, 8, 16, 32 times
Start Range : 1, 10, 100, 1000μA
Limiters : 2, 20, 200mA
◇ Sample points : 1 to 91 samples
◇ Measurement speed : Fast/slow
◇ Damage detection points : 1 to 10 points
◇ Damage criteria : Initial current * (1 to 100)%
+ (100nA to 1mA)

2. ESD pulse

◇ Polarity : Positive and Negative
◇ Period : About 1 sec
◇ Repetition : 1 to 100 times
◇ Charge Removal : Supported
◇ Zap voltage
HBM: 0 to 400V/5Vstep
400 to 4000V/50V step
MM: 0 to 400V/5V step
400 to 4000V/50V step
◇ Accuracy : 1% of setting±5V
◇ Waveform: MIL, JEDEC, JEITA, others

3. Test Program

◇ Semi-auto test
◇ Automatic test
◇ V/I curve measurement
◇ ESD zapping

* 10pA resolution may be available. Ask factory.

About Model 400SC

Host PC is not included in this picture.

Model 400SC is to test a die. The system zaps HBM, MM as well as F-CDM and D-CDM depending what probes you order. You may order TLP option as well to measure snap back curve by pulse curve tracer. Damage detection is not available for CDM tests.

◇ Meets MIL, JEDEC or JEITA standards
◇ X/Y stage motion : ±50mm
◇ Z axis motion : Less than 10mm

Specification subject to change without notice. Ask latest specification to:

More info to :