Universal Bench Top Unit

ESD and Pulse Technology

ESD/CDM Simulator Ecdm-100E/400E

6 Functions in a Compact Bench Top Unit

Field Induced CDM
Direct Charging CDM
HBM, Human Body Model
MM, Machine Model
TLP, Pulse Curve Measurement
Mobile Charge measurement
Wafer test available

Applications

- ESD Simulator
  - MR, GMR head
  - LCD panel
  - Small component, chip
  - Transistor, IC, Diode
- ESD noise immunity tester
  - LCD panel and driver
  - Assembled PC boar
  - Small unit
  - IC card, Memory card

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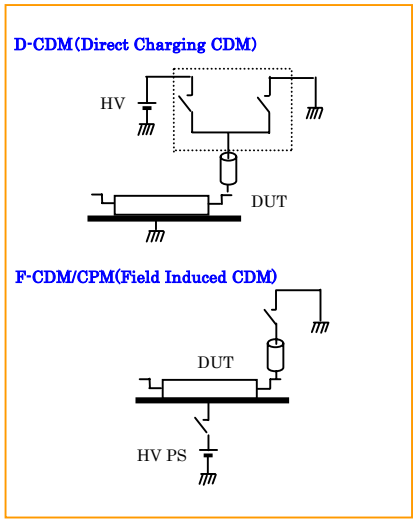
General



Electro-Static Discharge (ESD) is the major reason of the breakage, degradation or malfunction of the semiconductor devices, as design rule becomes more and more precise. The Model Ecdm-100E/400E is a bench top and manually operated simulator that allows ESD simulation such as Charged Device Model (CDM) discharge. To zap, touch the probe tip at DUT pin or PC board pattern, then depress the front panel switch or foot switch. It is easy to zap the location that is not flat. The Model Ecdm-100E/400E simulates both direct charge method and field-induced method of CDM. The direct charge method is major in Japan though field-induced method is mainly used in the US. The Model Ecdm-100E/400E simulates Human Body Model (HBM) and Machine Model (MM) as well, by replacing the probe, as an option. This is the only universal ESD simulator in the market.

The Ecdm-100E has two voltage ranges, 100V and 1000V and is useful to test the strength against ESD stress of the MR/GMR head, small chip component and LCD panel module. It is also useful to perform the ESD noise immunity test of the LCD panel, PC board and other module. Model Ecdm-400E has 400V and 4000V ranges and higher stress test is possible.

Ecdm series optionally equipped with a coulomb measurement probe that allows the charged or discharged amount of charge to/from the DUT that depends on the charged voltage. Recently, it has been found that this amount of charge that kills the DUT will decide the maximum allowable discharge level in the field so that it will not be damaged.

TLP (Transmission Line Pulse) configuration is available to verify the I/V curve as well as its robustness of the ESD protection circuit. Ask TLP literature if you need detail information of the TLP test.

Tokyo Electronics Trading Co. Ltd. (TET) has been developed fully automated ESD test system including CDM test system in these more than 10 years. The Model Ecdm-100/400E has been developed above this background, for the applications that is not suitable for the expensive and automated test system.

Specifications

- Standard Specifications

Zap Voltage: 0 to +/-100V or 1000V (Ecdm-100E)
: 0 to +/-400V or 4000V(Ecdm-400E)
Voltage display: Digital panel meter
Voltage programming: By Potentiometer
Voltage Range: 2 Ranges (Low/High by Switch)
Voltage resolution: 0.1V(100E), 1V(400E)
Polarity: Positive, Negative and Off
Repetitions: 1 to 99 or continuous
Output Enable : Push Switch
Wrist Strap terminal :Available
AC Power: 100V+/-10%, 200VA, 50/60Hz
Size, Weight: Mainbody 257W, 362D, 145H(mm),

- Options

Remote Control: GP-IB
Probes
① HBM Type E-3H(ESDA STD)
② MM Type E-7M)(ESDA STD)
③ D-CDM Type P-3A(Metal tool discharge model)
④ F-CDM Type P-4F)

- Jig/Others

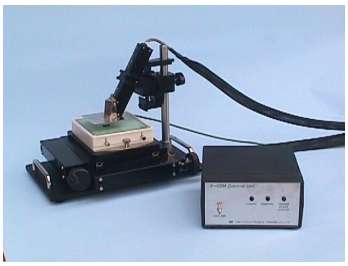
① Probe Mounting Stand Type ICJ-1
② X-Y Stage Type TST-1
③ DUT Jig: Made for each DUT
④ Needle Tip: 0.3, 0.5, 1.0 (mm)
⑤ Wafer test jig, Manipulator available

Options

HBM(E-3H) or MM(E-7M) Probe. Type name on case identify HBM or MM.
Automatic curve tracer connection after zap is available upon request.

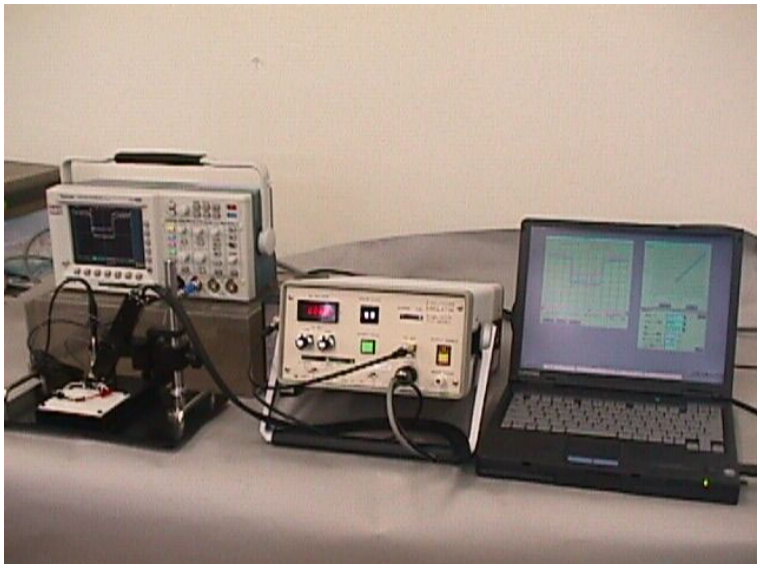
HBM or MM probe for wafer or die test. Model name on case identify HBM or MM probe.
Automatic curve tracer connection after zap is available upon request.

D-CDM probe (P-3A). 2 Types with upper ground plane (ESDA STD) and without upper ground plane (Metal tool discharge simulation) are available.

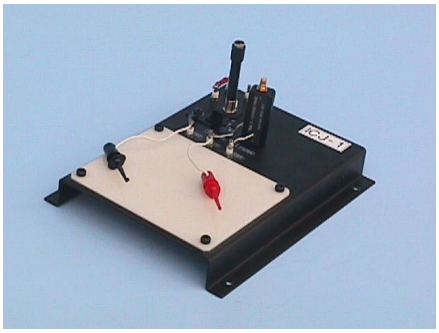


F-CDM probe (P-4F) and control box. Top ground plane size depend on the standard such as ESDA STD or JEDEC STD.
This picture shows Probe Mounting Stand (ICJ-1), X-Y stage, CDM base and DUT jig.

Mobile charge measurement probe (H-1KV) and nano-coulomb meter.
This picture shows Probe Mounting Stand (ICJ-1), X-Y stage, CDM base and DUT jig. CDM base and DUT jig are common for those of CDM test.



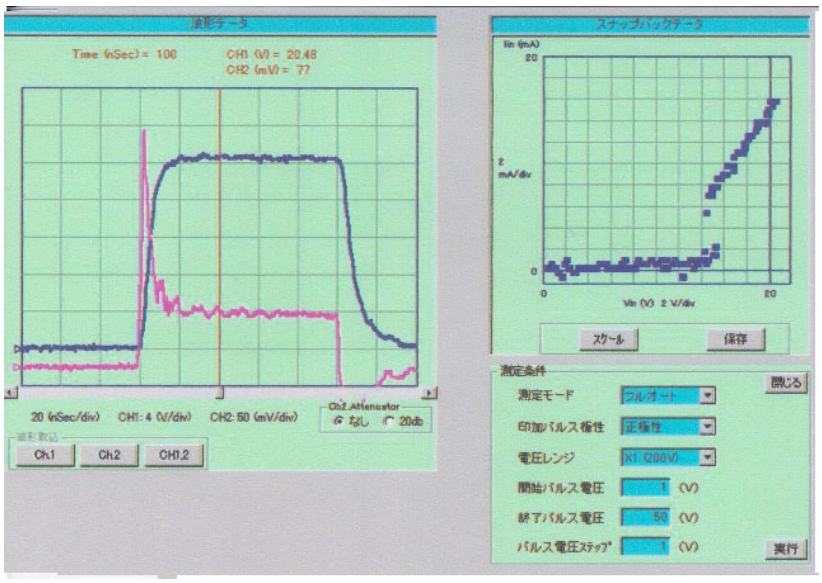
TLP Pulse Curve Tracer configuration



TLP test head

If Host PC controls the Model Ecdm-100E/400E-TLP via the optional GP-IB Interface, it allows the automatic I-V curve measurement for the ESD protection devices. This page describes an example of it.

Picture below shows an example of PC monitor.



Specification subject to change without notice.

Contact to: